SCHEME OF EXAMINATION
&
DETAILED SYALLBUS

for

Bachelor / Master of Technology (Dual Degree)
Information Technology

Guru Gobind Singh Indraprastha University
Kashmere Gate, Delhi [INDIA] –110 403
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SCHEME OF EXAMINATION

First Semester

Paper Code	ID	Paper	L	T/P	Credits
Theory Papers					
HS101	98101	Communication Skills-I	2	1	3
BA103	99103	Chemistry – I	2	1	3
IT105	15105	Introduction to Computers	3	-	3
IT107	15107	Electrical Science	3	1	4
BA109	99109	Mathematics – I	3	1	4
BA111	99111	Physics – I	2	1	3
HS119*	98119	Impact of Science & Technology on Society – I	1	-	1
Practical/Viva Voce					
BA151	99151	Chemistry-I Lab	-	2	1
BA153	99153	Physics-I Lab	-	2	1
IT155	15155	Computer Lab	-	2	1
IT157	15157	Engineering Graphics-I	-	2	1
IT159	15159	Electrical Science Lab	-	2	1
Total			**16**	**15**	**26**

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Second Semester

Paper Code	ID	Paper	L	T/P	Credits
Theory Papers					
HS102	98102	Communication Skills – II	1	2	3
IT104	15104	Engineering Mechanics	3	1	4
BA108	99108	Mathematics – II	3	1	4
BA110	99110	Physics-II	2	1	3
BA114	99114	Statistics Theory of Probability and Linear Programming	2	1	3
BA118	99118	Chemistry-II	2	1	3
HS126*	98126	Impact of Science & Technology on Society – II	1	-	1
IT128	15128	Data Structures	3	0	3
Practical/Viva Voce					
BA156	99156	Physics –II Lab	-	2	1
BA162	99162	Chemistry –II Lab	-	2	1
IT152	15152	Data Structure Lab	-	2	1
IT154	15154	Engineering Graphics-II lab	-	2	1
Total			**16**	**16**	**28**

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SCHEME OF EXAMINATION

Third Semester

Paper Code	ID	Paper	L	T/P	Credits
Theory Papers					
IT201	15201	Computational Methods	3	1	4
IT203	15203	Circuits and Systems	3	1	4
IT205	15205	Electronic Devices and Circuits	3	1	4
IT207	15207	Object Oriented Programming Using C++	3	1	4
IT209	15209	Computer Graphics	3	1	4
IT211	15211	Database Management Systems	3	1	4
Practical/Viva Voce					
IT251	15251	Electronic Devices and Circuits Lab.	-	2	1
IT253	15253	Computation Lab.	-	2	1
IT255	15255	Object Oriented Programming Lab.	-	2	1
IT257	15257	Computer Graphics Lab.	-	2	1
IT259	15259	DBMS Lab.	-	2	1
Total			**18**	**16**	**29**

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Fourth Semester

Paper Code	ID	Paper	L	T/P	Credits
Theory Papers					
IT202	15202	Java Programming	3	1	4
IT204	15204	Multimedia Applications	3	1	4
IT206	15206	Switching Theory and Logic Design	3	1	4
MS208	39208	Organization Behaviour	3	1	4
IT210	15210	Foundations of Computer Science	3	1	4
IT212	15212	Software Engineering	3	1	4
Practical/Viva Voce					
IT252	15252	Java Programming Lab.	-	2	1
IT254	15254	Multimedia Lab.	-	2	1
IT256	15256	Switching Theory and Logic Design Lab.	-	2	1
IT258	15258	Software Engineering Lab.	-	2	1
Total			**18**	**14**	**28**

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SCHEME OF EXAMINATION

Fifth Semester

Paper Code	ID	Paper	L	T/P	Credits
Theory Papers					
IT305	15305	Computer Architecture	3	1	4
IT307	15307	Digital Signal Processing	3	1	4
IT309	15309	Object Oriented Software Engineering	3	1	4
IT313	15313	Communication Systems	3	1	4
IT315	15315	Linux and Win32 Programming	3	1	4
IT317	15317	Operating Systems	3	1	4
Practical/Viva Voce					
IT353	15353	Digital Signal Processing Lab.	-	2	1
IT359	15359	Object Oriented Software Engineering Lab.	-	2	1
IT361	15361	Linux and Win32 Programming Lab.	-	2	1
IT357*	15357	Summer Training (Conducted at the end of the 4th Semester) Report, Seminar and Viva – Voce	-	-	1
Total			**18**	**12**	**28**

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Sixth Semester

Paper Code	ID	Paper	L	T/P	Credits
Theory Papers					
IT302	15302	Microprocessors	3	1	4
IT304	15304	Computer Networks	3	1	4
IT306	15306	Algorithm Analysis and Design	3	1	4
IT314	15314	Digital System Design	3	1	4
IT316	15316	Digital Communication	3	1	4
Practical/Viva Voce					
IT352	15352	Microprocessor Lab.	-	2	1
IT354	15354	Algorithm Analysis & Design Lab.	-	2	1
IT360	15360	DSD Lab.	-	2	1
IT362	15362	Digital Communication Lab.	-	2	1
Total			**15**	**13**	**24**

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Seventh Semester

Code	Paper ID	Paper	L	T/P	C
Theory Papers					
IT401	15401	Advanced Computer Networks	3	1	4
IT413	15413	Front End Design Tools and Web Technologies	3	1	4
Electives (Choose any two)					
IT403	15403	Software Testing	3	1	4
IT405	15405	Distributed Systems	3	1	4
IT415	15415	Advanced Java Programming	3	1	4
IT417	15417	Embedded System Design	3	1	4
IT419	15419	Wireless and Mobile Communication	3	1	4
IT421	15421	Data Warehousing and Mining	3	1	4
Practicals					
IT451	15451	ACN Lab.	-	2	1
IT453	15453	FEDT & Web Technology Lab.	-	2	1
IT455	15455	Laboratory Assignments	-	2	1
IT457	15457	Minor Project	-	-	5
IT459*	15459	Summer Training (Conducted at the end of the 6th Semester) Report, Seminar and Viva - Voce	-	-	1
Total			**12**	**10**	**25**

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Eighth Semester

Code	Paper ID	Paper	L	T/P	C
HS402*	98402	Technical Writing	2	-	2
Electives (Choose any two)					
IT404	15404	Advanced Computer Architecture	3	1	4
IT406	15406	Control Systems	3	1	4
IT408	15408	Advanced Database Management Systems	3	1	4
IT414	15414	Windows .Net Framework and C# Programming	3	1	4
IT416	15416	Mobile Computing	3	1	4
IT418	15418	Semantic Web	3	1	4
Practicals					
IT452	15452	Major Project (Report)	-	-	8
IT454	15454	Viva – Voce (On major project)	-	-	2
IT456*	15456	Seminar and progress report	-	-	1
IT458	15458	Laboratory Assignments	-	-	1
Total			**8**	**2**	**22**

***NUES**

Note:

1. '*' Marked papers are NUES papers.
2. Total number of credits in BTECH(IT) = 210
3. The minimum number of credits to be earned for the award of the degree is = 200
4. Papers from M.Tech. (2 years) programme may also be opted for IT/CSE/DCW.

Code: IT 305 **L:3 T/P:1 C: 4**

Paper ID: 15305 **Paper: Computer Architecture**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I

Computer Arithmetic and Register transfer language:

Unsigned notation, signed notation, binary coded decimal, floating point numbers, **IEEE 754 floating point standard**, Micro-operation, Bus and Memory Transfers, Bus Architecture, Bus Arbitration, Arithmetic Logic, Shift Micro operation, Arithmetic Logic Shift Unit.

Unit II

Instruction set architecture & computer organization

Levels of programming languages, assembly language instructions, **8085 instruction set architecture**, Instruction Codes, Computer Registers, Computer Instructions, Timing & Control, Instruction Cycle, Memory Reference Instructions, Input-Output and Interrupts

Unit III

Control Design:

Instruction sequencing & interpretation, Hardwired & Micro Programmed (Control Unit), Micrprogrammed computers, Micro coded CPU: Pentium processor

CPU Design

Specifying a CPU, Design & implementation of simple CPU, General Register Organization, Stack Organization, Instruction Formats, Addressing Modes, **Internal architecture of 8085 microprocessor**.

Unit IV

Memory organization

Memory Technology, Main Memory (RAM and ROM Chips), Virtual memory, High-speed memories

Input/Output organization

Asynchronous Data Transfers, Programmed I/O, interrupts, Direct memory Access, Serial communication, UARTs, **RS-232-C & RS-422** standard

Text:

1. J. D. Carpinelli, "Computer Systems Organization and Architecture", Pearson Education, 2006.
2. J. P. Hayes, "Computer Architecture and Organization", McGraw Hill, 1988.

Reference:

1. J. L Hennessy and D. A. Patterson, "Computer Architecture: A quantitative approach", Morgon Kauffman, 1992.
2. W. Stallings, "Computer organization and Architecture", PHI, 7th ed, 2005.
3. B. Parhami, "Computer Architecture: From Microprocessors to Supercomputers", Oxford University press, 2006.

Code: IT 307 **L:3 T/P:1 C: 4**

PaperID: 15307 **Paper : Digital Signal Processing**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**
1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.
2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I

Signals and signal Processing: Characterization & classification of signals, typical Signal Processing operations, example of typical signals, typical Signals Processing applications.

Time Domain Representation of Signals & Systems: Discrete Time Signals, Operations on Sequences, the sampling process, Discrete-Time systems, Time-Domain characterization of LTI Discrete-Time systems.

Unit II

Transform-Domain Representation of Signals: Discrete Fourier Transform (DFT), DFT properties, computation of the DFT of real sequences, Linear Convolution using the DFT. Z-transforms, Inverse z-transform, properties of z-transform.

Unit III

Computation of the Discrete Fourier Transform: Computational complexity of the direct computation of the DFT, different approaches for reducing the computations, Decimation-in-Time FFT algorithms, Decimation-in-frequency FFT algorithms.

Unit IV

Digital Filter Structure: Block Diagram representation, Signal Flow Graph Representation, Signal Flow Graph Representation, FIR Digital Filter Structure, IIR Filter Structures, Parallel all pass realization of IIR Filter design based on Frequency Sampling approach.

Text / Reference:

1. A. Y. Oppenhein and R. W. Schater, "Digital Signal Processing", PHI 1975.
2. Sanjit K. Mitra, "Digital Signal Processing: A Computer based approach", TMH, 2005.
3. J. G. Proakis and D.G. Manolakis, "Digital Signal Processing, Principals, Algorithms, and Applications", Pearson Education, 4th ed., 2007.
4. A. Y. Oppenhein, R. W. Schater and J. R. Buck, "Discrete Time Signal Processing", PHI 1999

Code No.: IT 309 **L:3 T/P:1 C: 4**
PaperID: 15309 **Paper: Object Oriented Software Engineering**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**
1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.
2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I

Introduction to Software Engineering: Software Engineering Development, Software Life Cycle Models, Standards for developing life cycle models.

Object Methodology & Requirement Elicitation: Introduction to object Oriented Methodology, Overview of Requirements Elicitation, Requirements Model-Action & Use cases, Requirements Elicitation Activities, Managing Requirements Elicitation.

Unit II

Architecture: Model Architecture, Requirements Model, Analysis Model, Design Model, Implementation Model, Test Model

Unit III

Modeling with UMLZ: Basic Building Blocks of UML, A conceptual Model of UML, Basic Structural Modeling , UML Diagram
System Design: Design concepts & activities, Design Models, Block design, Testing

Unit IV

Testing Object Oriented Systems: Introduction, Testing Activities & Techniques, The Testing Process, Managing Testing

Case Studies

Text Books:

1. I. Jacobson, "Object-Oriented Software Engineering: A Use Case Driven Approach", Pearson, 1992
2. B. Breugge and A. H. Dutoit, "Object Oriented Software Engineering: Using UML, Patterns, and Java", Prentice Hall, 2004.
3. G. Booch, J. Rumbaugh and I. Jacboson, "The Unified Modeling Language User Guide" Addison-Wesley, 2005

Code No.: IT 313 **L:3 T/P:1 C: 4**

Paper ID: 15313 **Paper: Communication Systems**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I

Classification of signals & systems, Fourier Series, Fourier transforms and their applications to system analysis. Representations of random signals, Concept of Probability, Probability distribution Function, Probability density Function, Gaussian, Binomial, Raleigh and Poisson's distribution, Random Process, Correlation Function, Power Spectral Density, Response of Linear systems to random signals. Gaussian distribution, Central Limit theorem, Ergodicity, co-variance.

Unit II

Concepts of Modulation, Various Analog modulation and demodulation techniques (AM, FM, PM). Multiplexing,

Unit III

Analog to Digital Conversion, Various pulse modulation techniques (PAM, PPM, PWM & PCM). Delta Modulation.

Unit IV

Introduction to Information Theory & Noise: Introduction, Noise its sources, mathematical representation of noise, noise temperature, S/N ratio & Noise figure. Measure of Information, Channel Capacity, Bandwidth S/N trade off.

Text:

1. W. Tomasi, "Electronic communications systems(baics through advanced)", Pearson Education, 2th ed, 2004.
2. H. Taub and D. L. Schilling, "Principles of Communication Systems", TMH, 1992.

Reference:

1. J. C. Hancock, "An Introduction to the Principles of Communication Theory", McGraw Hill, 1961.
2. S. Haykins, "Introduction to Analog and Digital Communication", Wiley, 1986.
3. G. Kennedy and B. Davis, "Electronic communication systems", TMH, 1993.
4. J. G. Proakis, M. S.alehi, "Communications Systems Engineering", PHI, 2nd ed, 2002.
5. D. Roddy and J. Coolen, "Electronic Communications", PHI, 1995.
6. S. Haykins, "Communication Systems", Wiley, 2001.

Code: IT 315 **L:3 T/P:1 C: 4**

Paper ID: 15315 **Paper: Linux & Win32 Programming**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Linux:

Unit I

Linux overview, Compiler options, libraries, make, file system objects, error handling, I/O, file locking, manageing files, directory management, temporary files and cleanup, command line processing.

Unit II

UserID, password and group management; signals, and signal handling, process management, fork and exec, regular expression, IPC, message queues, semaphores, shared memory, memory mapped files, Introduction to X-Windows.

Win32:

Unit III

Windows environment, Windows programming options, Windows and messages, text, controls, keyboard management, Mouse management, Timer, Child window controls, Menus and other resources, Dialog boxes, Clipboard management

Unit IV

GDI, Printer management, Bitmaps and Bitblts, Device Independent Bitmaps, Palette manager, Metafiles, Multiple Document Interface, Introduction to MFC.

Text:

1. K. Wall, M. Watson, and M. Whitis, " Linux Programming Unleashed", SAMS, 1999.
2. C. Petzold, "Programming Windows: The definitive guide to Win32 API", Microsoft Press, 5th Eds., 1998.

Code No.: IT 317 **L C**

Paper ID: 15317 **Paper: Operating System** **4 4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I.

Introduction to the Operating System

Types of OS: Batch System, Time Sharing System, Real Time System, Multiuser/Single User System

Functions of Operating System: Process Management, Memory Management, File Management, I/O Devices Management, Information Management.

Process Management : Process concepts, Process State, Process Control Block, Process Scheduling, Context Switch, CPU Scheduling, Scheduling Criteria, Scheduling Algorithms, Pre Emptive/ Non Preemptive Scheduling, Threads, Thread Structure.

Unit II

Process Synchronisation: Critical Section Problem, Race Condition, Synchronisation Hardware, Semaphores, Classical Problems of Synchronisation.

Dead Locks: Characterisation, Methods for Handling Deadlocks Avoidance, Recovery and Detection.

Unit III

Memory Management: Contiguous Allocation, External Internal Fragmentation, Paging, Segmentation, Segmentation with Paging.

Unit IV

Virtual Memory: Virtual Memory Concepts, Access Methods, Directory Structure, allocation Methods; Contiguous Allocation, Linked Allocation, Indexed Allocation Free Space Management.

Device Management: dist Structure, Disk Scheduling Algorithms, Disk Management, Case study on DOS, Windows 2000, Windows XP, Linux.

Text:

1. Silbershatz and Galvin, “Operating Systems Concepts”, Addition Weseley, 2002
2. Flynn, Mchoes, “Understanding Operating System”, Thomson Press, Third Edition, 2003
3. Godbole Ahyut, “Operating System”, PHI, 2003

References:

1. Charles Crowley, “Operating Systems, Tata Mcgraw-Hill Edition.
2. A.S. Tannenbaum, “Operating System Concepts”, Addition Weseley, 2002

Code No.: IT 302 **L:3 T/P:1 C: 4**

Paper ID: 15302 **Paper: Microprocessors**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I

Introduction – Microprocessors Evolution and types (Intel 4004 – Pentium IV and road maps), Overview of 8085, 8086, 80286, 80386, 80486, Pentium processors and Micontrollers.

Unit II

Architecture of 8086 – Register Organization, Execution unit, Bus Interface Unit, Signal Description, Physical Memory Organization, General Bus Operation, I/O addressing capabilities, Minimum mode and maximum mode timing diagrams, Comparison with 8088

Unit III

8086 programming – Assembly language program development tools (editor, linker, loader, locator, Assembler, emulator and Debugger), Addressing modes, Instruction set descriptions, Assembler directives and operators, Procedures and Macros. (Writing programs for use with an assembler MASM)

Unit IV

8086 Interfacing – Interfacing 8086 with semiconductor memory, 8255, 8254/ 8243, 8251, 8279, A/D and D/A converters. Numeric processor 8087, I/O processor 8089 tightly coupled and loosely coupled systems.

Text:

1. D.V. Hall, "Microprocessors and Interfacing", TMH, 2nd Ed. 1991.
2. Y.-C. Liu and G. A. Gibson, "Microprocessor Systems: The 8086/8088 family Architecture, Programming & Design", PHI, 2000.

References:

1. J. L. Antonakes, "An Introduction to the Intel Family of Microprocessors", Thomson, 1996.
2. K. J. Ayala, "The 8086 microprocessor", Thomson, 1995
3. Peter Able, "IBM PC assembly language programming", PHI, 2000.
4. A. K. Ray and K M Bhurchandi, "Advanced Microprocessors and Peripherals", TMH, 2000.

Paper Code: IT 304 **L:3 T/P:1 C: 4**

PaperID:15304 **Paper: Computer Networks**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I

Introduction: Uses of Computer Networks, Network and Protocol Architecture, Reference Model (ISO-OSI, TCP/IP-Overview

Physical Layer: Data and signals, Transmission impairments, Data rate limits, performance factors, Transmission media, Wireless transmission, Telephone system (Structure, trunks, multiplexing & Switching)

Unit II

Data Link Layer: Design issues, Error detection & correction, Data Link Protocols, sliding window protocols, HDLC,WAN Protocols.

Unit III

Medium Access Sub layer: Channel allocation problem, multiple access protocols, IEEE standard 802.3 & 802.11 for LANS and WLAN, high-speed LANs, Network Devices-repeaters, hubs, switches bridges.

Unit IV

Network Layer: Design issues, Routing algorithms, congestion control algorithms, Internetwork protocols, Internetwork operation

Text :

1. B. A Forouzan.,"Data Communications & Networking",4th Ed, Tata McGraw Hill, 2007.
2. A. S. Tanenbaum. "Computer networks", Pearson Education, 4th ed , 2006.

References:

1. W. Stallings, "Data and Computer Communications", Pearson Education, 8th Ed, 2007.
2. D. E. Comer., "Computer Networks & Internets", Pearson Education, 4th Ed, 2007
3. N. Olifer and V. Olifer, "Computer Networks", Wiley, 2006
4. L. L. Peterson and B. S. Davie, "Computer Networks",Elsevier,4th Ed, 2007.
5. L. A. Gallo, "Computer Communications & networking technologies", Cengage Learning, India 1st Ed, 2007.

Code: IT 306 **L:3 T/P:1 C: 4**

Paper ID: 15306 **Paper: Algorithm Analysis and Design**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I

Growth of Functions, Summations, Algorithm Design Paradigms, Sorting in Linear Time: Counting sort, Radix Sort, Bucket Sort, Medians and Order Statistics, Disjoint Set operations, Linked List representation of disjoint sets, disjoint set forests.

Unit II

Matrix Chain Multiplication, Strassen's algorthim for matrix multiplication, LCS, Optimal Binary Search Tree, General Greedy approach Vs Dynamic Programming approachm Case studies: Knapsack problem, Huffman Coding Problem, Matroids

Unit III

Representation of Graphs, Breadth First Search, Depth First Search, Topological Sort, Strongly Connected Components, Algorithms of Kruskal's and Prim's, Dijkstra's and Bellman ford algorithm, All pair shortest path, Flyod Warshall Algorithm

Unit IV

String Matching: The Naïve String Matching Algorithm, The Rabin Karp Algorithm, String Matching with Finite Automata, The Knuth Morris Pratt Algorithm.

NP-Complete Problems: Polynomial Time Verification, NP-Completeness and Reducibility, NP Completeness proof, NP-Complete Problems.

Text:

1. T .H . Cormen, C . E . Leiserson, R .L . Rivest, "Introduction to Algorithms", PHI, 2001.

References:

1. A .V. Aho, J . E . Hopcroft, J . D . Ulman "The Design & Analysis of Computer Algorithms", Addison Wesley, 1998.
2. U . Manber "Introduction to Algorithms – A Creative Approach", Addison Wesley, 1998.
3. E. Horwitz and S. Sahani "Fundamentals of Computer Algorithms", Galgotia, 1998.
4. P. Linz, "An Introduction to Formal Languages and Automata", Narosa Publishing House, 2000.
5. J.E.Hopcroft and J.D.Ullman, "Introduction to Automata Theory, Languages and Computation", Addison Wesley, 1998.
6. K.L.Mishra & N.Chandrasekaran, "Theory of Computer Science", PHI,1996.
7. John C.Martin, "Introduction to Languages and Theory of Computation", TMH, 2001.

Code: IT 314 **L:3 T/P:1 C: 4**

Paper ID: 15314 **Paper: Digital System Design**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I

Introduction to HDLs, Design Flow, Synthesis, VHDL Basics, Data types, Operators, Concurrent coding, Structural and Behavioural Modelling, Design of Adder, Substractor, Decoder, encoder, Code converter, Multiplexer, VHDL for Combinational Circuits, Blocks, Generate Statements.

Unit II

Sequential Code, Control Structure, Attributes, VHDL for Flip Flops, Design of Shift Registers & Counters using VHDL, Design of memory using VHDL, Signals and Variable.

Unit III

VHDL timing, modelling with Delta time Delays, Inertial/Transport Delay, Packages and Libraries, Function, Procedure, Resolution Function, Operator Overloading, RTL systems: Organization of systems, Data Subsystem, Control Subsystem.

Unit IV

Testing and the Test Bench: Manufacturing Testing, Functional Testing, Test Benches, VHDL Test Bench, Files and Text I/O.

Programmable Logic Arrays (PLAs), PALs, Study of architecture of FPGA and CPLD, Case study of FPGA device Virtex 5 family.

Text:

1. C. H. Roth, "Digital System Design using VHDL", Thomson Learning 2005
2. V. A. Pedroni, "Circuit Design with VHDL", PHI, 2005

References:

1. B. Cohen, "VHDL coding Styles and Methodologies", Springer, 2005
2. J F Wakerly, "Digital Design Principles and Practice" , Pearson Education Press 2007
3. S. Ghose, "Hardware Description Languages", PHI 2005
4. P.J. Ashendern, "The Designer Guide to VHDL", Morgan Kaufmann, 2005
5. D J Smith , "HDL Chip Design", Don Publisher, 2005
6. D. L. Perry, "VHDL programming", TMH, 2005
7. K.C. Chang and M Loeb, "Digital Systems Design with VHDL and Synthesis", Wiley, 2005
8. J. Bhaskar , "A VHDL Synthesis Primer", BSP, 2006.
9. J. Bhaskar, "A VHDL Primer", Pearson Education, 2005
10. S. Lee, "Advanced Digital Logic Design Using VHDL, State Machines, and Synthesis for FPGA's", Morgan Kaufmann, 2007
11. B. Vransesic, "Fundamental of Digital Logic Design with VHDL", TMH, 2007.

Code: IT 316 **L:3 T/P:1 C: 4**

Paper ID: 15316 **Paper: Digital Communication**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.

2. Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks

Unit I

PULSE MODULATION

Sampling process – PAM – other forms of pulse modulation – Bandwidth – Noise trade off – Quantization –PCM –Noise considerations in PCM Systems – TDM – Digital multiplexers – Virtues, Limitation and modification of PCM – Delta modulation – Linear prediction – Differential pulse code modulation – Adaptive delta Modulation.

Unit-II

BASEBAND PULSE TRANSMISSION

Matched Filter – Error Rate due to nose – Intersymbol Interference – Nyquist's criterion for Distortionless Base band Binary Transmission – Correlative level coding – Baseb and M -ary PAM transmission – Adaptive Equalization – Eye patterns.

Unit III

PASSBAND DATA TRANSMISSION

Introduction – Pass band Transmission model – Generation, Detection, Signal space diagram, bit error probability and Power spectra of BPSK, QPSK, FSK and MSK schemes – Differential phase shift keying -Comparison of Digital modulation systems using a single carrier – Carrier and symbol synchronization.

Unit IV

ERROR CONTROL CODING

Discrete memoryless channels – Liner block codes – Cyclic codes – Convolutional codes – Maximum, likelihood decoding of convolutional codes – Viterbi Algorithm, Trellis coded Modulation, Turbo codes.

SPREAD SPECTRUM MODULATION

Pseudo – noise sequences – a notion of spread spectrum – Direct sequence spread spectum with coherent binary phase shift keying – Signal space Dimensionality and processing gain – Probability of error – frequency – hop spread spectrum – Maximum length and Gold codes.

Text:

1. Simon Haykins, "Communication Systems" John Wiley, 4th Edition, 2001

References:

1. Sam K. Shanmugam "Analog and Digital Communication " John Wiley, 2002.
2. John G.Proakis, "Digital Communication" McGraw Hill 3rd Edition,1995.
3. H. Taub and D. L. Schilling, "Principles of Communication Systems", TMH, 2003.